IN THE DRAWINGS

Please amend FIGS. 1a, 1b, 2, 4 and 6 as shown in the redline versions attached hereto, and enter the enclosed replacement sheets for those figures as originally filed.

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REMARKS

Claims 1-6, 8-13, 15-21, and 23-32 are pending. Claims 7, 14, 22, 25 and 29 have been canceled. Claims 1, 5, 8-9, 15, 18, 21, 23, 26, and 30 have been amended. No new matter has been introduced. Reexamination and reconsideration of the present application are respectfully requested.

In the Office Action dated June 29, 2005, the Examiner objected to the drawings under 37 C. F. R. §§ 1.84 (n) and 1.84 (o). Applicants have amended FIGS. 1A 1B, 2, 4, and 6 in view of the Examiner's comments and have enclosed herewith redline versions of these figures. In addition, Applicants have enclosed replacement sheets for the aforementioned amended drawing figures in accordance with 37 C. F. R. § 1.84. Accordingly, Applicants respectfully submit that the objection should be withdrawn.

The Examiner objected to claim 1 because of informalities. Applicants have amended claim 1 in view of the Examiner's comments. Accordingly, Applicants respectfully submit that the objection should be withdrawn.

The Examiner rejected claims 1-21 and 23-32 under 35 U.S.C. § 112, first paragraph as failing to comply with the written description requirement. The Examiner is correct in stating that the data sample and phase sample are derived from the input data as is disclosed in Applicants specification with reference to FIG. 3. Applicants have amended claims 1, 5 and 23 to clarify this point in view of the Examiner's comments. Accordingly Applicants respectfully submit that the rejection should be withdrawn.

The Examiner rejected claims 1-4 and 18-21 under 35 U.S.C. § 112, second paragraph, as being indefinite. Applicants have amended claims 1 and 18 in view of the Examiner's comments. Applicants respectfully submit that the claims 1-4 and 18-21 are definite and

accordingly submit that the rejection should be withdrawn.

The Examiner rejected claim 22 under 35 U.S.C. § 102(b) as being anticipated by LaRosa et al., U.S. Patent No. 5,247,544 (hereinafter LaRosa). The Examiner rejected claims 5-7 and 10-13 under 35 U.S.C. § 103(a) as being unpatentable over Masenas et al., U.S. Patent No. 6,614,316 (hereinafter Masenas) in view of Hill, U.S. Patent No. 6,031,428 (hereinafter Hill). The Examiner rejected claim 9 under 35 U.S.C. § 103(a) as being unpatentable over Masenas in view of Hill and Perrott et al., U.S. Patent No. 6,630,868 (hereinafter Perrott). The Examiner rejected claim 17 under 35 U.S.C. § 103(a) as being unpatentable over Masenas in view of Hill and Ogawa, U.S. Patent No. 5,574,757 (hereinafter Ogawa). The Examiner rejected claims 18-21 under 35 U.S.C. § 103(a) as being unpatentable over Hill in view of Roberts et al., U.S. Patent No. 6,735,259 (hereinafter Roberts). The Examiner rejected claims 23-25 and 28 under 35 U.S.C. § 103(a) as being unpatentable over LaRosa in view of Masenas and Hill. The Examiner rejected claim 27 under 35 U.S.C. § 103(a) as being unpatentable over LaRosa in view Masenas and Hill and in further view of Perrott. The Examiner rejected claim 32 under 35 U.S.C. § 103(a) as being unpatentable over LaRosa in view of Masenas and Hill and in further view of Ogawa. Applicants respectfully traverse the rejections in view of the claims as amended.

Independent claim 5, as amended now recites:

A timing recovery system to receive input data having a phase, comprising:
a phase locked loop to lock a phase of a local clock to the phase of said input data, said phase locked loop receiving said input data and generating a phase locked loop output, wherein said phase locked loop includes:
a phase detector to determine said phase of said input data, said phase detector receiving said input data and generating a phase detector output; and
a loop filter to provide an additional frequency characteristic to said phase detector output, said loop filter receiving said phase detector output and generating said phase locked loop output;
a first proportional path with non-linear control to adjust the phase of said input data in response to a data pattern of said input data, said first proportional path receiving said input data and generating a first proportional path output;

a second proportional path with non-linear control to adjust the phase of said input data in response to an amplitude of data samples derived from said input data, said second proportional path receiving said input data and generating a second proportional path output;

a system summing node, wherein said phase locked loop output, said first proportional path output, and said second proportional path output are summed by said system summing node to generate a system summing node output;

a data density detector to monitor a density of said input data, said data density detector receiving said input data and generating a data density detector output; and

a frequency detector to determine a frequency of an incoming timing jitter of said input data, said frequency detector receiving said phase detector output and generating a frequency detector output.

The Masenas reference does not disclose, teach or suggest the system specified in independent claim 5, as amended. As the Examiner has acknowledged, Masenas does not teach a second proportional path with non-linear control to adjust the phase of said input data in response to an amplitude of data samples derived from said input data, said second proportional path receiving said input data and generating a second proportional path output. *(June 29 Office Action, page 5)*

In addition, unlike the system specified in claim 5, the Masenas reference does not teach a system that includes "***a data density detector to monitor a density of said input data, said data density detector receiving said input data and generating a data density detector output.***" Instead the Masenas reference is directed to controlling loop dynamics of a frequency synthesizer. *(Masenas; Col. 1, lines 7-9)* Masenas discloses a timing recovery system which generates a phase error estimate and controls loop dynamics of a frequency synthesizer without using external components. *(Masenas; Col. 2, lines 51-62)* However, Masenas fails to disclose or suggest "***a data density detector to monitor a density of said input data, said data density detector receiving said input data and generating a data density detector output***" Accordingly, Applicants respectfully submit that independent claim 5 distinguishes over Masenas.

The Hill reference does not make up for the deficiencies of Masenas. The Hill reference is directed to a Steered Frequency Phase Locked Loop. *(Hill; Abstract)* Hill discloses a system for providing an accurate clock in the event of a clock signal failure. *(Hill; Col. 2, lines 12-20)* However, the combination of the Hill and Masenas does not disclose, teach, or suggest "***a data density detector to monitor a density of said input data, said data density detector receiving said input data and generating a data density detector output.***" Accordingly, Applicants respectfully submit that independent claim 5 distinguishes over Masenas in combination with Hill.

Independent claims 18 and 23, as amended recite limitations similar to those in independent claim 5. Accordingly, Applicants respectfully submit that claims 18 and 23 distinguish over Masenas in combination with Hill for reasons similar to those set forth above with respect to claim 5.

Claims 6, 8-13, and 15-17 depend from independent claim 5, as amended. Claims 19-21 depend from independent claim 18, as amended. Claims 24, 26-28, and 30-32 depend from independent claim 23. Accordingly, Applicants respectfully submit that claims 6, 8-13, 15-17, 19-21, 24, 26-28, and 30-32 distinguish over Masenas in combination with Hill for the same reasons set forth above with respect to claim 5.

With respect to claims 9 and 27, the Perrott reference does not make up for the deficiencies of Masenas and Hill. The Perrott reference is directed to clock and data recovery circuits. *(Perrott; Col 1, lines 16-19)* Perrott discloses a phase locked loop 140 which includes a digital integrating block 152 having a digital accumulator 156. The digital accumulator 156 takes a digital phase error representation from an A/D converter which receives an analog phase error output signal from phase detector 142, and

increases or decreases the cumulative value. *(Perrott; Col. 5, lines 25-50)* Nevertheless, the combination of Massenas, Hill and Perrott does not disclose, teach, or suggest "***a data density detector to monitor a density of said input data, said data density detector receiving said input data and generating a data density detector output.***" Accordingly, Applicants respectfully submit that independent claims 9 and 27 distinguish over Masenas in combination with Hill and Perrott.

With respect to claim 17, the Ogawa reference does not make up for the deficiencies of Masenas and Hill. Ogawa discloses a phase locked loop circuit including a hold off counter. *(Ogawa; FIG 2)* However, the combination of Massenas, Hill and Ogawa does not disclose, teach, or suggest "***a data density detector to monitor a density of said input data, said data density detector receiving said input data and generating a data density detector output.***" Accordingly, Applicants respectfully submit that independent claim 17 distinguishes over Masenas in combination with Hill and Ogawa.

With respect to claims 18-21, the Roberts reference does not make up for the deficiencies of Hill. Roberts discloses estimation of phase error based on a data sample from an optimum timing Topt of input data. *(Roberts; Col. 9, lines 16-28)* However the combination of Hill and Roberts does not disclose, teach, or suggest "***a data density detector to monitor a density of said input data, said data density detector receiving said input data and generating a data density detector output.***" Accordingly, Applicants respectfully submit that claims 18-21 distinguish over Hill in combination with Roberts.

With respect to claims 23-25 and 28, the LaRosa reference does not make up for the deficiencies of Masenas and Hill. The LaRosa reference is directed to a clock recovery circuit and a method for adjusting the phase of a recovered clock signal.

(LaRosa; Abstract) LaRosa discloses a phase adjustment circuit that automatically holds the clock phase during periods of poor channel quality. The clock recovery scheme generates a sampling clock which is synchronous with the received signal and generates at least two error signals which indicate the quality of the received signal at different sampling phases. A normalized error signal is generated by comparing each error signal with the smallest received error signal and processed to determine the desired phase of the sampling clock signal. *(LaRosa; Col. 2, lines 25-46)* However the combination of LaRosa, Masenas and Hill does not disclose, teach, or suggest "***a data density detector to monitor a density of said input data, said data density detector receiving said input data and generating a data density detector output.***" Accordingly, Applicants respectfully submit that claims 23-25 and 28 distinguish over LaRosa in combination with Masenas and Hill.

With respect to claim 27, the LaRosa reference does not make up for the deficiencies of Masenas, Hill and Perrott. As noted above, LaRosa discloses a clock recovery circuit and a method for adjusting the phase of a recovered clock signal. However, the combination of LaRosa, Masenas, Hill, and Perrott does not disclose, teach, or suggest "***a data density detector to monitor a density of said input data, said data density detector receiving said input data and generating a data density detector output.***" Accordingly, Applicants respectfully submit that claim 27 distinguishes over LaRosa in combination with Masenas, Hill, and Perrott.

With respect to claim 32, the LaRosa reference does not make up for the deficiencies of Masenas, Hill and Ogawa. The combination of LaRosa, Masenas, Hill, and Ogawa does not disclose, teach, or suggest "***a data density detector to monitor a***

density of said input data, said data density detector receiving said input data and generating a data density detector output." Accordingly, Applicants respectfully submit that claim 27 distinguishes over LaRosa in combination with Masenas, Hill, and Perrott.

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Applicants believe that the claims are in condition for allowance. If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 488-7100 to discuss the steps necessary for placing the application in condition for allowance should the Examiner believe that such a telephone conference call would advance prosecution of the application.

Respectfully submitted,

PILLSBURY WINTHROP SHAW PITTMAN LLP

Date: October 18, 2005

By: _____

Roger R. Wise
Registration No. 31,204
Customer No. 27496

725 South Figueroa Street, Suite 2800
Los Angeles, CA 90017-5406
Telephone: (213) 488-7100
Facsimile: (213) 629-1033